Abstract of the Disclosure

This invention provides a micro controller in which JTAG port becomes available through a specific operation even after a security bit is set. More specifically, this invention provides a micro controller wherein: when an address signal AD2 and data DT2 are input from JTAG port 11, the address signal AD2 and data DT2 are kept in shift registers 25 and 26 through TAP 24; the address signal AD2 is forwarded to flash ROM and data DT1 of the address specified by the address signal AD2 is read out and output a comparator 27; the data DT2 is also output the comparator 27; when the data DT1 and DT2 agree, the output signal from the comparator 27 turns "H" and the output signal from the AND 23 turns "L" independent of security signal SEQ; and hereby the JTAG control circuit 12 turns switch-on and the JTAG port 11 becomes connected to the TAP 13 and 14 through the JTAG control circuit 12.